CLAIMS

What is claimed is:

1. A method comprising:

creating a plurality of rows of via holes through a circuit board substrate from a first surface of the substrate to a second surface of the substrate;

forming a conductive layer on the first surface and on the second surface;

forming a conductive path through each of the via holes from the first surface to the second surface; and

severing the substrate through each row of via holes and between each row of via holes along a coordinate axis, to produce a plurality of elongate substrate members.

2. A method as recited in claim 1, further comprising coupling at least one of the elongate substrate members between an electronic component package and a circuit board.

3. A method as recited in claim 1, further comprising affixing two or more of the elongate substrate members together to form an interposer.

4. A method as recited in claim 3, wherein said affixing comprises affixing two or more of the elongate substrate members together to form an interposer configured with an array of via holes.

5. A method as recited in claim 4, further comprising coupling the interposer between an electronic component package and a circuit board.

6. A method as recited in claim 1, further comprising forming a plurality of elongate grooves in the first surface and in the second surface of the substrate, prior to said severing.

7. A method as recited in claim 1, wherein said grooves are formed parallel to each other between rows of via holes.

8. A method of manufacturing an interposer, the method comprising:

creating a plurality of rows of via holes through a circuit board substrate from a first surface of the substrate to a second surface of the substrate, the first surface and the second surface being coated with a conductive material;

forming a conductive layer in each of the via holes to provide a conduction path through each of the via holes from the conductive material on the first surface to the conductive material on the second surface;

selectively removing some of the conductive material from the first surface and the second surface to form a plurality of traces on the first surface and the second surface, each trace in electrical contact with the conductive layer in at least one of the via holes; and

severing the substrate to produce a plurality of individual substrate members, by cutting the substrate through the middle of the via holes in each

row of via holes and between each row of via holes along a particular axis.

9. A method as recited in claim 8, further comprising affixing two or more of the plurality of individual substrate members together to form an interposer as a substantially planar array.

10. A method as recited in claim 9, further comprising coupling the interposer between an electronic component package and a circuit board.

11. A method as recited in claim 10, wherein the electronic component package includes a semiconductor die, and wherein the circuit board is a motherboard.

12. A method as recited in claim 8, further comprising forming grooves in the first surface and the second surface of the substrate between the via holes.

13. A method as recited in claim 8, wherein the conductive coating is a surface layer applied in each of the via holes.

14. A method as recited in claim 8, further comprising coupling at least one of the individual substrate members between an electronic component package and a circuit board.

15. A method of manufacturing an interposer, the method comprising:

creating a plurality of via holes through a circuit board substrate from a first surface of the substrate to a second surface of the substrate; and

creating a solid conductive column through each of the via holes, the conductive column forming an electrical path from the first surface to the second surface.

16. A method as recited in claim 15, further comprising coating the first surface and the second surface with a conductive material.

17. A method as recited in claim 16, further comprising selectively removing some of the conductive material from the first surface and the second surface to form a plurality of traces on the first surface and the second surface, each trace in electrical contact with the conductive column of one of the via holes.

18. A method as recited in claim 15, further comprising forming grooves in the first surface and the second surface of the substrate between the via holes.

19. A method as recited in claim 15, further comprising coupling the interposer between an electronic component package and a circuit board.

20. A method as recited in claim 19, wherein the electronic component package includes a semiconductor die and the circuit board is a motherboard.

21. A method as recited in claim 15, wherein each of the conductive columns has a composition of tin (Sn) and lead (Pb).

22. A method as recited in claim 21, wherein the composition comprises at least

81% lead (Pb).

23. A method of manufacturing an interposer, the method comprising:

creating a plurality of via holes through a circuit board substrate from a first surface of the substrate to a second surface of the substrate;

creating a conductive path through each of the via holes from the first surface to the second surface; and

forming a plurality grooves in the first surface and the second surface of the substrate between the via holes.

24. A method as recited in claim 23, wherein said forming a plurality grooves comprises:

forming a first plurality of grooves in the first surface of the substrate;

forming a second plurality of grooves in the first surface of the substrate, perpendicular to the first plurality of grooves;

forming a third plurality of grooves in the second surface of the substrate;

forming a fourth plurality of grooves in the second surface of the substrate, perpendicular to the third plurality of grooves.

25. A method as recited in claim 23, further comprising selectively removing some of the conductive material from the first surface and the second surface to form a plurality of traces on the first surface and the second surface, each trace in electrical contact with the conductive column of one of the via holes.

26. A method as recited in claim 23, wherein said creating a conductive path through each of the via holes comprises forming a thin conductive layer on a surface of each of the via holes.

27. A method as recited in claim 26, further comprising severing the substrate to produce a plurality of elongate beams, by cutting the substrate through the middle of the via holes in each row of via holes and between each row of via holes along a particular axis.

28. A method as recited in claim 27, further comprising affixing two or more of the plurality of beams together in an array configuration to form the interposer.

29. A method as recited in claim 23, wherein said creating a conductive path through each of the via holes comprises forming a solid conductive column through each of the via holes.

30. A method as recited in claim 23, wherein each of the conductive columns has a composition of tin (Sn) and lead (Pb).

31. A method as recited in claim 30, wherein the composition comprises at least 81% lead (Pb).

32. A method as recited in claim 23, further comprising coupling the interposer between an electronic component package and a circuit board.